User Manual

GHD1440T

200V Half-Bridge Gate Driver

Version: V1.0

Contents

1 Product Overview

1.1 Introduction

GHD1440T is a single-phase medium-voltage high-speed gate drive IC, which is specially designed for driving double-N-channel VDMOS power transistor or IGBT in bridge circuits, and is suitable for application schemes for motor drive and DC-DC conversion.

The embedded typical dead time is 230ns. When the dead time of the MCU output signal is less than the embedded dead time, the actual dead time is the embedded dead time. On the contrary, when the dead time of the MCU output signal is greater than the embedded dead time, the actual dead time is the output dead time of MCU. The embedded VCC and VBS undervoltage protection functions can prevent the system from turning on the external power transistors at low driving voltage. The output of the high-side driving circuit and the output of the low-side driving circuit are controlled through input signals respectively.

1.2 Main characteristics

- Operating range of supply voltage: 5.5~20V
- Floating offset voltage: 200V
- Embedded typical dead time value is 230ns
- Embedded VCC/VBS undervoltage protection
- Embedded straight-through prevention function
- Embedded input bias resistor
- Embedded output bias resistor
- Matching the transmission time of high and low-end channels
- High dv/dt noise suppression capability
- High-end output and input are non-inverting
- Low-end output and input are inverting
- Compatible with 3.3V/5V logic input
- Embedded bootstrap diode
- Peak output source current 1.6A@15V, 3.3nF load fall time 35ns
- Peak output sink current 1.3A@15V, 3.3nF load rise time 55ns

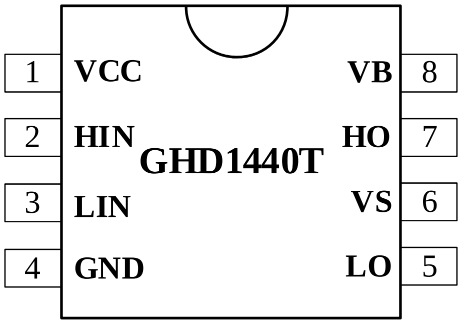
1.3 Application scope

- Motor drive
- DC-DC converter

2 Pin Information

2.1 Pin distribution

Figure 1 Distribution Diagram of GHD1440T Pins



2.2 Pin functional description

Table 1 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definitions
Pin type	P	Power pin or ground
	I	Input pin
	O	Output pin
	I/O	I/O pin

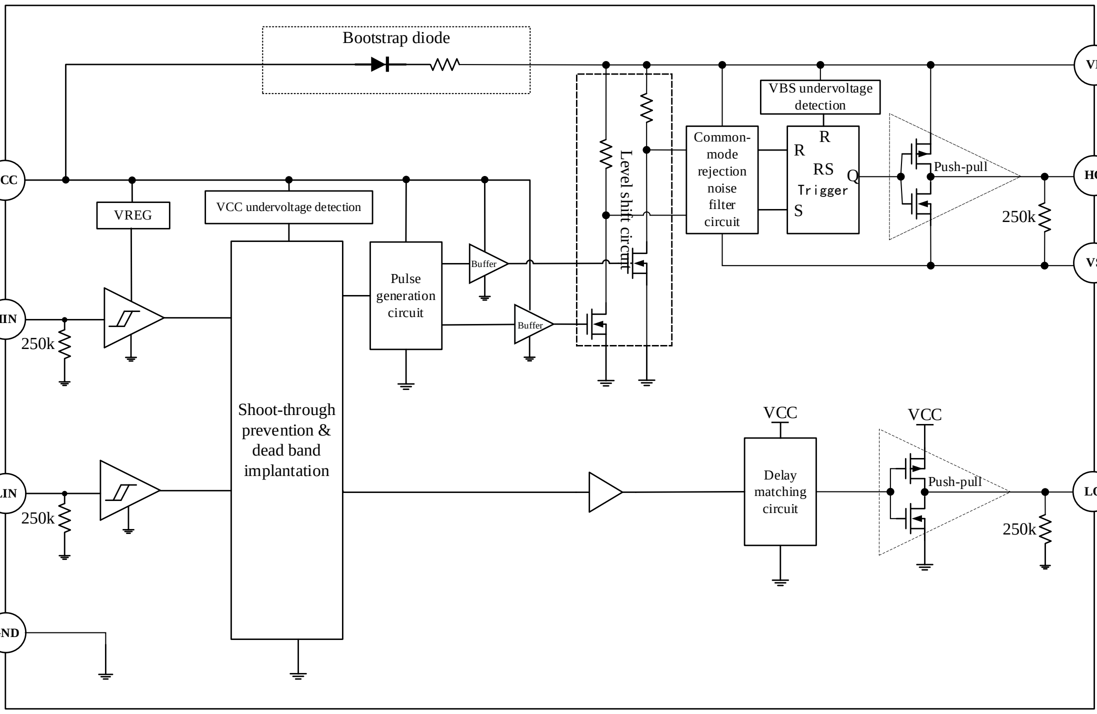
Table 2 GHD1440T Pin Description

Name	Type	Functional description	Pin sequence
VCC	P	Power terminal	1
HIN	I	High-side input	2
LIN	I	Low-side input	3
GND	P	Ground terminal	4
LO	O	Low-side output	5
VS	P	High-side floating end	6
HO	O	High-side output	7
VB	P	High-side boot power end	8

3 System Block Diagram

3.1 Internal block diagram

Figure 2 GHD1440T Internal Block Diagram



3.2 Logic truth value

Table 3 Logic Truth Value

VCCUV	VBSUV	LIN	HIN	LO	HO
normal	normal	L	H	L	L
normal	normal	H	L	L	L
normal	normal	L	L	H	L
normal	normal	H	H	L	H
normal	UV	H&L	H&L	L&H	L
UV	normal	H&L	H&L	L	L

Notes:

(1) VBS undervoltage will only pull the HO output low;

(2) VCC undervoltage will pull both LO and HO outputs low.

4 Electrical Characteristics

4.1 Recommended safe operating range

Unless otherwise specified, T_A= 25°C, and all pins take GND as the reference point.

Table 4 General Operating Conditions

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
T_A	Ambient temperature	-40	-	105	℃
V_{HO}	High-side output voltage	VS	VS+15	VB	V
V_{LO}	Low-side output voltage	0	15	VCC	V
VB	High-side floating offset absolute voltage	VS+5.5	VS+15	VS+20	V
VS	High-side floating offset relative voltage	-5	-	140	V
VCC	Supply voltage	5.5	15	20	V
V_{IN}	Input voltage (HIN/LIN)	0	-	5	V

Note:

(1) When VB=VS+10, and VS is in the range of (GND-5V) to (GND-VBS), the HO logic state is maintained. When VS is in the range of (GND-5V) to 140V, the HO operates normally.

(2) Operation beyond the recommended conditions for a long time may affect its reliability.

4.2 Absolute maximum rated value

Unless otherwise specified, T_A= 25°C, and all pins take GND as the reference point.

Table 5 Power Consumption

Symbol	Description	Minimum value	Maximum value	Unit
P_D	Maximum power consumption	-	0.6	W

Note: At any time, the power consumption cannot exceed P_D. The calculation formula for the maximum power consumption at different ambient temperatures is: P_D=(150℃-T_A)/θ_{JA}, wherein 150℃ is the maximum operating junction temperature of the circuit, T_A is the operating ambient temperature of the circuit, and θ_{JA} is the thermal resistance of the package.

Table 6 Temperature Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
T_s	Storage temperature	-55	150	℃
θ_{JA}	Junction-to-ambient thermal resistance	-	200	℃/W
T_J	Junction temperature	-	150	℃
T_L	Pin welding temperature (duration 10s)	-	260	℃

Table 7 Maximum Rated Current Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{HO}	High-side output voltage	VS-0.3	VB+0.3	V
V_{LO}	Low-side output voltage	-0.3	VCC+0.3	V
VB	High-side floating offset absolute voltage	-0.3	225	V
VS	High-side floating offset relative voltage	VB-25	VB+0.3	V
VCC	Supply voltage	-0.3	25	V
V_{IN}	Input voltage (HIN/LIN)	-0.3	12	V
dVS/dt	Maximum slew rate of offset voltage	-	50	V/ns

Table 8 ESD Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{ESD}	Electrostatic discharge voltage (human body model)	-	1000	V

Note: The 100pF capacitor is discharged through a 1.5kΩ resistor.

4.3 Electrical characteristic parameters

Unless otherwise specified, T_A=25°C, VCC=VBS=15V, VS=GND, and all pins take GND as the reference point.

Table 9 Supply Current Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{CCQ}	VCC quiescent current	V_{HIN}=0V, V_{LIN}=5V	240	300	550	μA
I_{BSQ}	VBS quiescent current	V_{HIN}=0V, V_{LIN}=5V	25	30	50	μA
I_{CCD}	VCC dynamic current	f_{LIN}=20kHz	350	500	800	μA
I_{BSD}	VBS dynamic current	f_{HIN}=20kHz	100	180	250	μA
I_{LK}	VB floating power supply leakage current	V_{IN}=float, VB=225V	-	-	10	μA

Table 10 Supply Voltage Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
VCC_{HY+}	VCC undervoltage positive threshold		3.5	4.5	5.4	V
VCC_{HY-}	VCC undervoltage negative threshold		3.4	4.3	5.1	V
VCC_{HY}	VCC undervoltage hysteresis		-	0.2	-	V
VBS_{HY+}	VBS undervoltage positive threshold		3.3	4.2	5.0	V
VBS_{HY-}	VBS undervoltage negative threshold		2.8	4.0	4.8	V
VBS_{HY}	VBS undervoltage hysteresis		-	0.2	-	V
VS_{QN}	VS static negative pressure	VBS=15V	-5	-	-	V

Table 11 Input-end Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IN+}	High-level input voltage		1.6	-	-	V
V_{IN-}	Low-level input voltage		-	-	2.1	V

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{INHY}	Input hysteresis voltage		-	0.3	-	V
I_{IN+}	High-level input voltage	V_{HIN}=5V, V_{LIN}=0V	15	20	30	μA
I_{IN-}	Low-level input current	V_{HIN}=0V, V_{LIN}=5V	-	-	1	μA

Table 12 Output-end Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{OUT+}	High-level output voltage	I_{OUT}=20mA (difference from power supply)	70	120	220	mV
V_{OUT-}	Low-level output voltage	I_{OUT}=20mA (difference from ground)	30	60	120	mV
I_{OUT+}	High-level short-circuit pulse current	V_{IN}=5V V_O=0V PWD≤10μS	0.7	1.3	1.9	A
I_{OUT-}	Low-level short-circuit pulse current	V_{IN}=0V V_O=15V PWD≤10μS	0.9	1.6	2.2	A

Table 13 Time Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
T_{ON}	Output rising edge transmission time	No Load	115	160	260	ns
T_{OFF}	Output falling edge transmission time	No Load	115	160	260	ns
T_R	Output rise time	C_L=3.3nF	35	55	95	ns
T_F	Output fall time	C_L=3.3nF	25	35	70	ns
DT	Dead time	No Load	160	230	320	ns
MDT	Dead band match time	No Load	-	-	50	ns
MT	High and low-side match time	No Load	-	-	50	ns

Table 14 Bootstrap Parameters

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{BSD15L}	Bootstrap charging current	VCC=15V, VB=13V	10	14	20	mA

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
I_{BSD15H}	Bootstrap charging current	VCC=15V, VB=0V	70	90	110	mA

5 Description of Application

5.1 Recommended application circuit diagram

Figure 3 Application Circuit

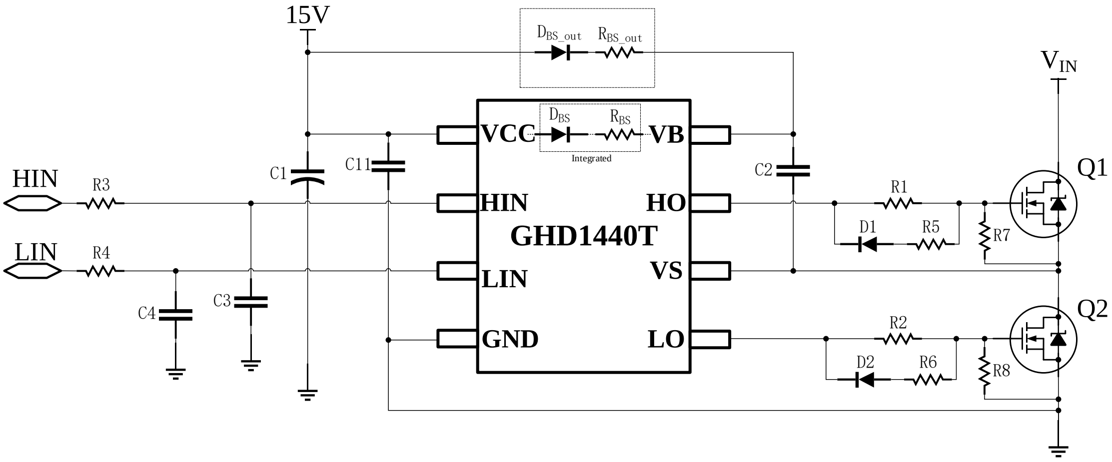


Table 15 Recommended Parameters

Device list	Name	Recommended application value	Recommended package
C1	Power storage capacitor	100F/50Vμ	Electrolytic capacitor
C11	Power filter capacitor	1F/50Vμ	Chip capacitor 1206
C2	Bootstrap energy storage capacitor	2.2F/50V (depending on the application)μ	Chip capacitor 1206
C3, C4	Input filter capacitor	1nF/16V	Chip capacitor 0603
R3, R4	Input filter resistor	100Ω/5%	Chip resistor 0603
R1, R2	Output driver resistor	30Ω/1% (depending on the application)	Chip resistor 0603
R5, R6	Driver fast-closing resistor	3.3Ω/1% (depending on the application)	Chip resistor 0603
D1, D2	Driver fast-closing diode	1N4148	SOD323
R7, R8	Gate pull-down resistor	100kΩ	Chip resistor 0805
D_{BS_OUT}	Bootstrap diode (external)	Select reverse breakdown voltage (>225V)	SMB
R_{BS_OUT}	Bootstrap current-limiting resistance (external)	10 Ω	Chip resistor 0805

Note:

(1) Power storage capacitor C1, which requires a relatively large capacitance to ensure power supply stability.

(2) Power supply filter capacitor C11, with a capacitance value smaller than that of C1, to filter power supply noise;

(3) The output driver resistors R1/R2 are determined by the parameters of the driven device, dead time, MOSFET power consumption, and electromagnetic compatibility. It is recommended to use the backward diode fast-closing or PNP triode fast-closing circuit;

(4) R3/C3 and R4/C4 are input RC filtering circuits, which can filter signal noise;

(5) The bootstrap capacitor C2 should select a voltage resistance of 2×VCC or above, and a capacitance value within 1u~100uF. It shall be selected based on the actual observed ripple, and be used in conjunction with a clamping diode;

(6) R5/D1 and R6/D2 constitute a fast-closing circuit, which can improve the shutdown speed and optimize the parasitic conduction noise;

(7) The bootstrap diode D_{BS_OUT} with fast recovery is recommended, with a voltage resistance of 1.5*VIN or above and an instantaneous current value greater than 1A. It shall be used in conjunction with a current limiting resistor according to the actual power-on and charging time.

5.2 PCB layout suggestions

(1) The chip-powered filter capacitor C11 is placed nearby between the VCC pin and GND pin, and the bootstrap current limiting resistor R_{BS_OUT}, bootstrap diode D_{BS_OUT}, and bootstrap capacitor C_2 are placed nearby at the corresponding pin of IC to minimize the circuit area;

(2) Minimize the routing length between the PWM output and the IC PWM input, and place the filter RC components R3, C3, R4, C4 close to the IC pins;

(3) Place the output driver resistors R1, R2 and driver fast-closing resistors R5, R6 close to the gates Q1, Q2, to reduce the oscillation caused by routing inductance on the drive signal;

(4) The area of the power circuit should be as small as possible, and the power ground, power supply ground, and signal ground should be routed separately;

(5) If a DC-DC switching power supply is used in the circuit, the operating frequency of the DC-DC circuit should be high, and the circuit area

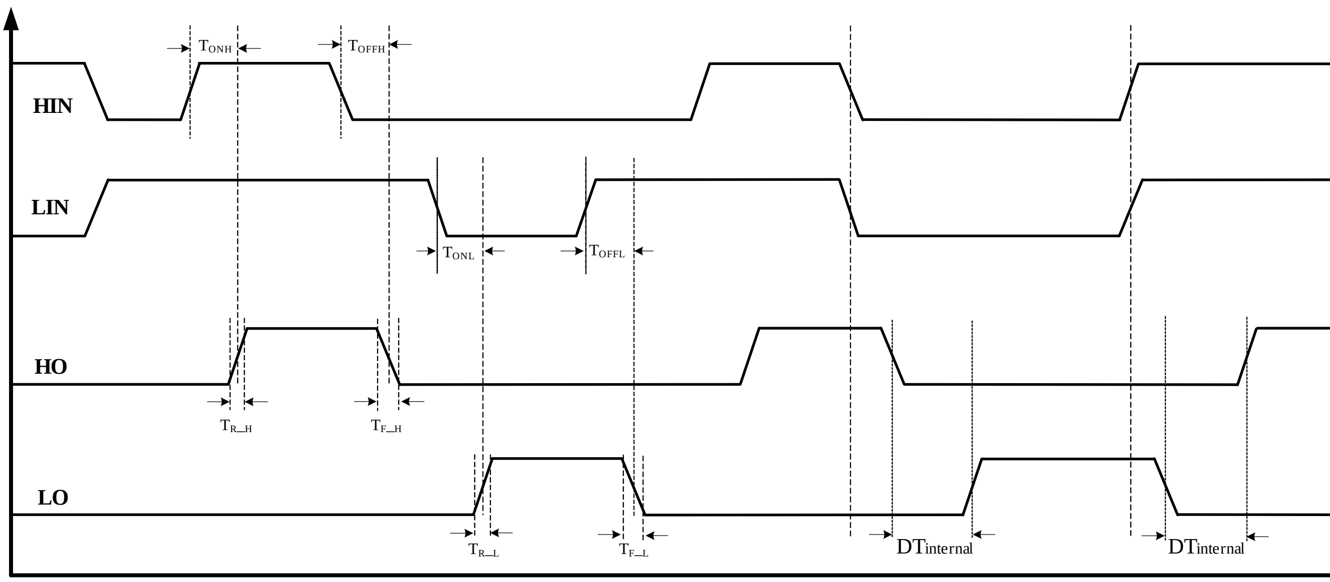
should be as small as possible. It is best to arrange this part according to the recommended layout for the used DC-DC chip.

6 Test Instructions

6.1 Time parameter test

The time parameters mainly include the output rise time t rise , the output fall time t fall , the rising edge transmission time t on , the falling edge transmission time t off , and the dead time DT.

Figure 4 Time Parameters



6.2 VCC/VBS undervoltage test

VCC is the low-side power supply, and VBS is the high-side power supply.

To prevent the system from turning on external power transistors at low drive voltage, an undervoltage locking circuit is embedded. The VCC undervoltage high and low values fall into the level trigger type, the VBS undervoltage high value falls into the edge trigger type, the HIN edge retrigger is required, and the VBS undervoltage low value falls into the level trigger type.

Figure 5 VCC Undervoltage Timing Diagram (ignoring transmission delay)

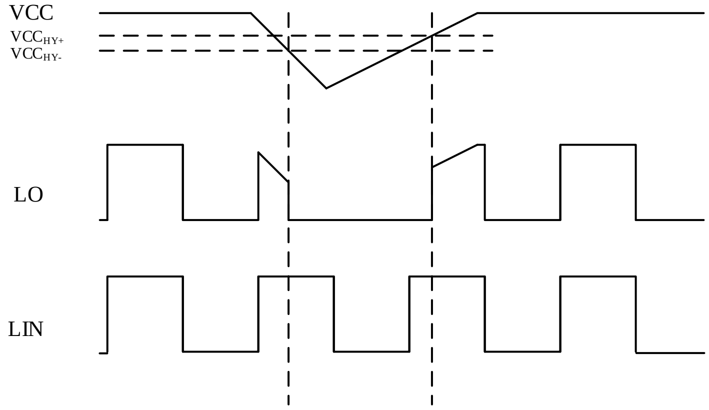
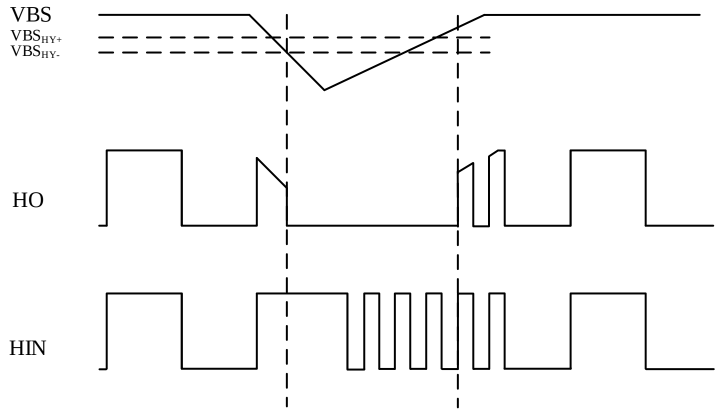


Figure 6 VBS Undervoltage Timing Diagram (ignoring transmission delay)

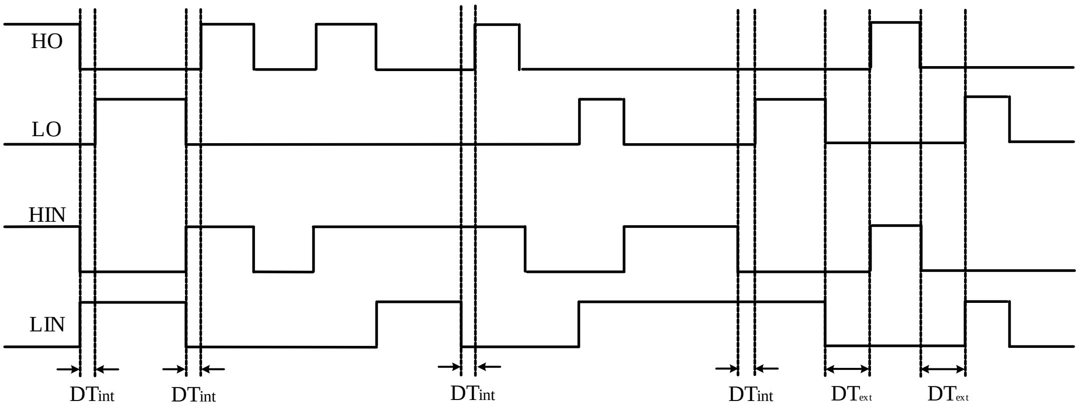


6.3 Straight-through protection and dead time test

A straight-through protection and dead time protection circuit based on the input signal is embedded in the chip. The double high level on the input logic will be determined as a straight-through signal, and the corresponding output will be set to low; moreover, it ensures that at least one dead time is embedded between the output high levels under any input condition. The logic of the external dead time DText given on the input end and the embedded dead time DTint is as follows:

- If $DT_{ext}>DT_{int}$，$DT=DT_{ext}$
- If $DT_{ext}<DT_{int}$，$DT=DT_{int}$

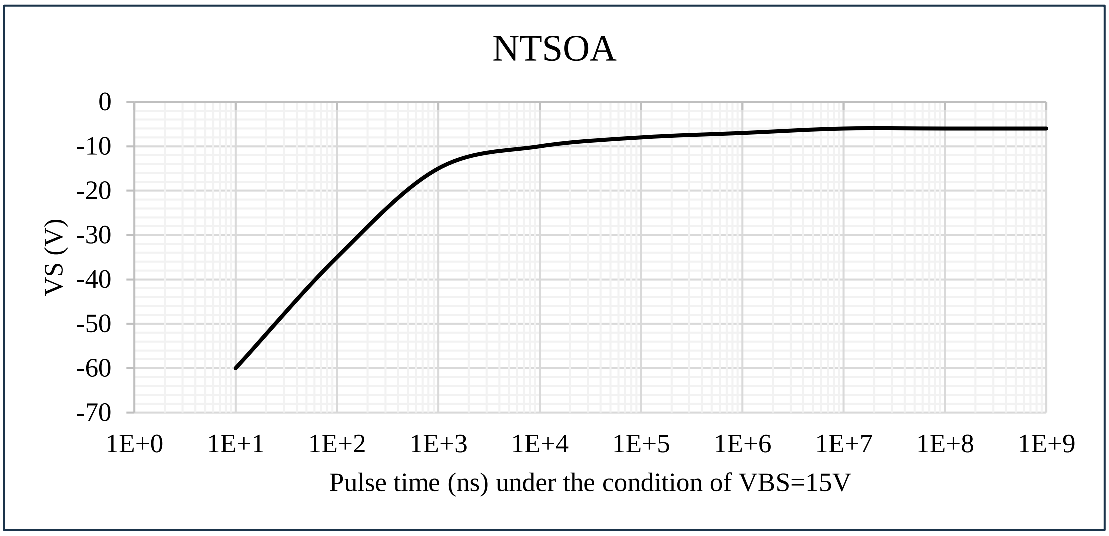
Figure 7 Logic Timing Diagram (ignoring transmission delay)



6.4 Transient negative-voltage safe operation area

The transient negative-voltage safe operating area (NTSOA) is used to characterize the capability of the gate driver to handle transient negative voltage. Typically, for negative pulses that fall within the area above the transient negative-voltage safe operating area boundary, the gate driver can avoid failure. It is recommended to actually leave sufficient margin. The negative pulses that fall within the area above the transient negative-voltage safe operating area boundary may cause the gate driver to malfunction or even become permanently damaged.

Figure 8 Transient Negative-voltage Safe Operation Area



7 Package Information

7.1 SOP8 package diagram

Figure 9 SOP8 Package Diagram

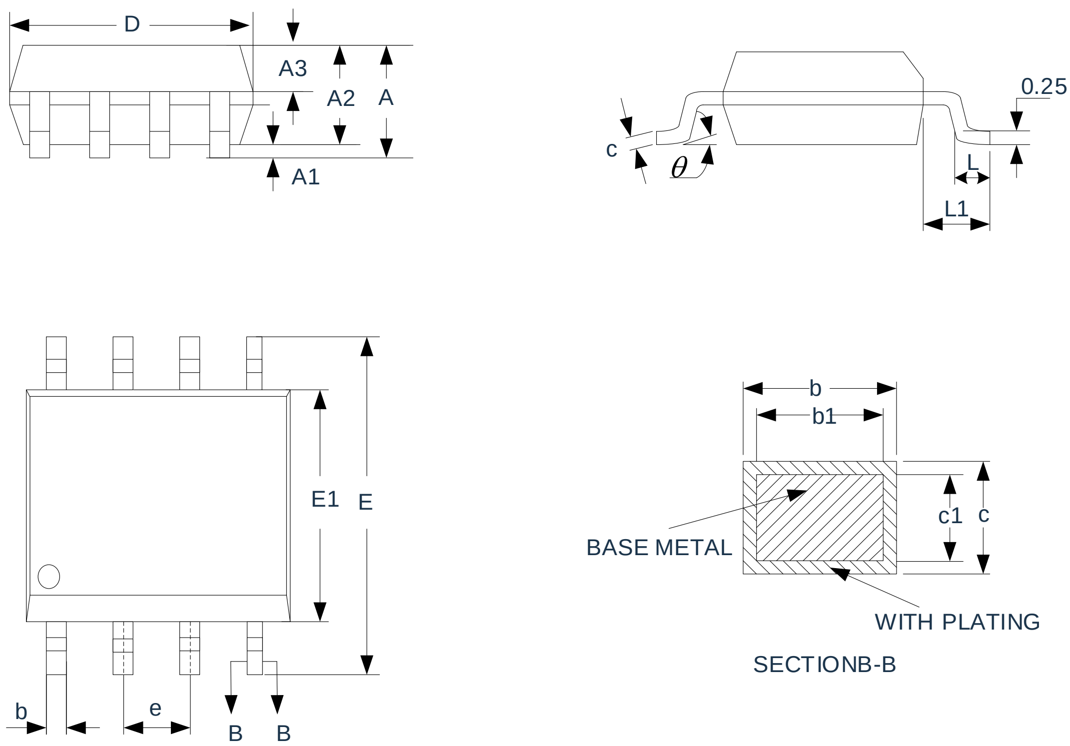


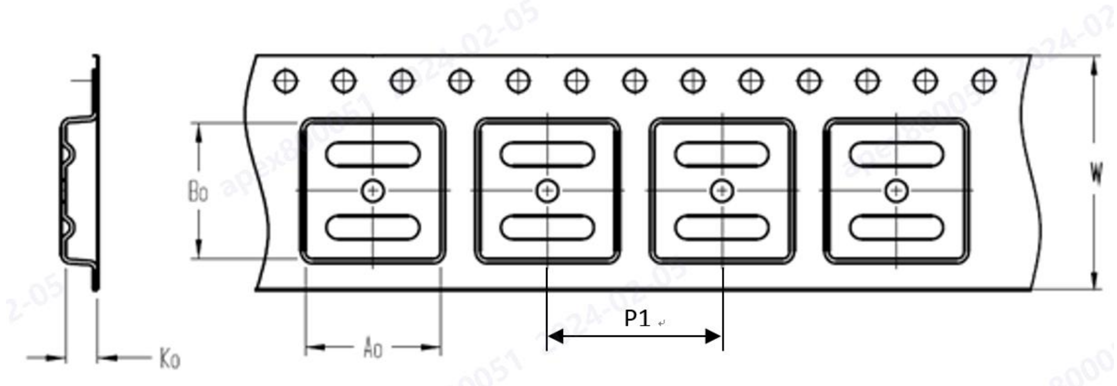
Table 16 SOP8 Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	--	0.48
b1	0.38	0.41	0.43
c	0.21	--	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	--	8°

8 Packaging Information

8.1 Reel Packaging

Figure 10Tape Dimensions



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
P1	Dimension designed to accommodate the component pitch
W	Overall width of the carrier tape

Figure 11 Quadrant allocation in PIN1 direction in tape

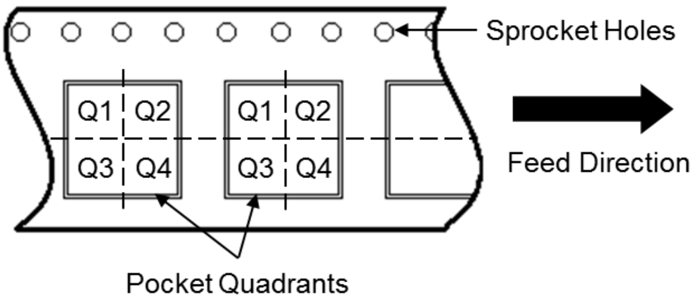


Figure 12 Reel Dimensions

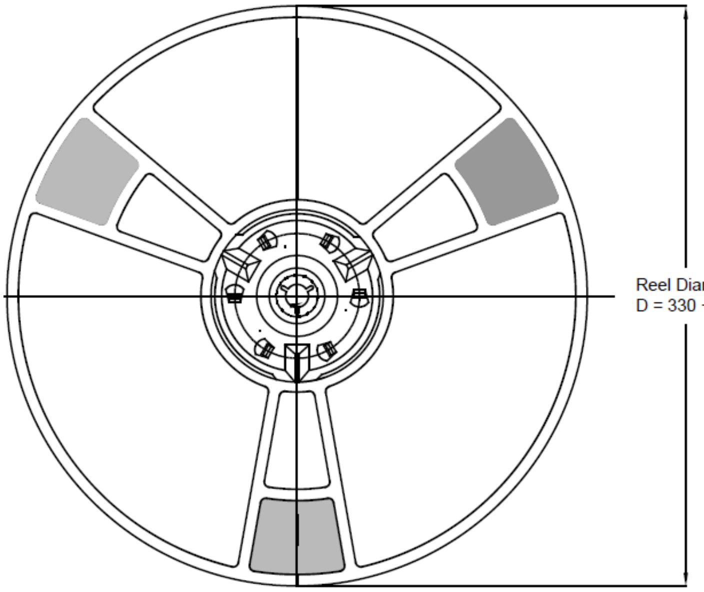


Table 17 Tape packaging parameter specification table

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	P1 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
GHD1440T	SOP	8	8000	13	6.55	5.3	4	2	12	Q1

9 Ordering Information

Table 18 Ordering Information

Product model	Package	Packaging	SPQ	Temperature range
GHD1440T	SOP8	Reel	8000	-40℃~105℃

10 Revision History

Table 19 Revision History

Date	Version	Revision History
2026.4	V1.0	● Initial version

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